CLAIMS:

What is claimed is:

1. An apparatus comprising:

a processor handling an I/O request in an I/O operation;

main storage controlled by the processor for storing data;

one or more I/O devices for sending data to or receiving data from said main storage;

a vector mechanism operable to register I/O requests by said devices to send or receive data from said main storage;

a dispatcher operable to poll said vector mechanism to determine if there is an outstanding I/O request; and

an override bit having a first condition when an immediate interrupt is to be sent to said processor for handling an I/O request from said I/O device(s), and a second condition when said dispatcher is to poll said vector mechanism to determine if there is an outstanding I/O request, said override bit being set to its first condition or reset to its second condition by said processor.

2. The apparatus of claim 1 further comprising a Target Delay Interval (TDI) register containing a TDI value for determining when the vector mechanism should not be polled by said dispatcher and an interrupt given to said processor, and wherein said overide bit, when in its first condition,overides said TDI value and drives an immediate interrupt to said processor.

3. The apparatus of claim 1 wherein said main storage is divided into multiple partitions, with each partition having a vector mechanism operable to register I/O requests by said devices to send or receive data from that partition of main storage, each partition having an associated override bit for that partition, and said processor is a hypervisor for setting the override bit for that partition when said hypervisor is to handle an immediate interrupt rather than polling by said dispatcher for that partition.

4. The apparatus of claim 3 further comprising one or more central processing units (CPUs) assignable by said hypervisor to one or more of said partitions, said hypervisor further setting the override bit of one partition when that partition does not have a CPU assigned to it.

5. The apparatus of claim 1 wherein said override bit is reset to its second condition after an interrupt is handled by said processor.

6. The apparatus of claim 5 wherein said override bit is reset to its second condition after said dispatcher polls said vector mechanism, said resetting of said override bit to its second condition upon the first to occur of said interrupt handling or said dispatcher polling.

7. An apparatus controlling the transfer of data in a data processing system having a processor handling an I/O request in an I/O operation, main storage controlled by the processor for storing data, and one or more I/O devices for sending data to or receiving data from said main storage, said apparatus comprising:

a vector mechanism operable to register I/O requests by said devices to send or receive data from said main storage;

a dispatcher operable to poll said vector mechanism to determine if there is an outstanding I/O request;

an override bit having a first condition when an immediate interrupt is to be sent to said processor for handling an I/O request from said I/O device(s), and a second condition when said dispatcher is to poll said vector mechanism to determine if there is an outstanding I/O request, said override bit being set to its first condition or reset to its second condition by said processor.

8. The apparatus of claim 7 further comprising a Target Delay Interval (TDI) register containing a TDI value for determining when the vector mechanism should not be polled by said dispatcher and an interrupt given to said processor, and wherein said overide bit, when in its first condition,overides said TDI value and drives an immediate interrupt to said processor.

9. The apparatus of claim 7 wherein said main storage is divided into multiple partitions, with each partition having a vector mechanism operable to register I/O requests by said devices to send or receive data from that partition of main storage, each partition having an associated override bit for that partition, and said processor is a hypervisor for setting the override bit for that partition when said hypervisor is to handle an immediate interrupt rather than polling by said dispatcher for that partition.

10. The apparatus of claim 9 further comprising one or more central processing units (CPUs) assignable by said hypervisor to one or more of said partitions, said hypervisor further setting the override bit of one partition when that partition does not have a CPU assigned to it.

11. The apparatus of claim 7 wherein said override bit is reset to its second condition after an interrupt is handled by said processor.

12. The apparatus of claim 11 wherein said override bit is reset to its second condition after said dispatcher polls said vector mechanism, said resetting of said override bit to its second condition upon the first to occur of said interrupt handling or said dispatcher polling.

13. A method for controlling the transfer of data in a data processing system having a processor handling an I/O request in an I/O operation, main storage controlled by the processor for storing data, and one or more I/O devices for sending data to or receiving data from said main storage, said method comprising:

registering in a vector mechanism, I/O requests by said devices to send or receive data from said main storage;

polling with a dispatcher, said vector mechanism to determine if there is an outstanding I/O request; and

sending an immediate interrupt to said processor when an override bit has a first condition for handling an I/O request from said I/O device(s), or polling with said dispatcher, said vector mechanism to determine if there is an outstanding I/O request when said overide bit is in a second condition.